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ThinkCentre User Guide Types 8086, 8087, 8088 Types 8089, 8090... Page 3 ThinkCentre User Guide Types 8086, 8087, 8088 Types 8089, 8090... Page 4. Before using this information and the product it supports, be sure to read the "Important safety information" on page v and Appendix E, "Notices," on page 45.

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2. When the 8088 ready to release the system bus, it will use RQ \bar{A} /GT \bar{A} 0 as an output to inform the new bus master. A second low level one period pulse does this. 3. The 8088 enters a Hold ACK state until the new bus master is ready to give the bus back by sending a third low level one period pulse as an input.

Week 7 The 8088 and 8086 Microprocessors

bus request (\bar{A} hold \bar{A}) to the 8088 (pulse 1). 2. During a T4 or T1 clock cycle, a pulse one clock wide from the 8088 to the requesting master (pulse 2), indicates that the 8088 has allowed the local bus to float and that it will enter the \bar{A} hold acknowledge state at the next CLK.

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